Abstract of the Disclosure

There is provided a fuse detection circuit comprising a first PMOS transistor (P3) having a source and drain connected between a power supply potential and a first node (A), and a gate connected with a control signal; a fuse mounting section having one terminal a connected to the first node (A) and the other end b connected to a drain of a first NMOS transistor (N4); the first NMOS transistor (N4) having the drain and a source connected between the other end b and a ground potential, and a gate connected with the control signal; a second PMOS transistor (P4) having a source and drain connected between the power supply potential and a second node (B), and a gate connected with the control signal; a reference resistance having one end connected to the second node (B) and the other end connected to a drain of a second NMOS transistor (N5); the second NMOS transistor (N5) having the drain and a source connected between the other end of the reference resistance and the ground potential and a gate connected with the control signal; a first inverter circuit comprising a PMOS transistor (P2) and an NMOS transistor (N2) connected in series between the power supply potential and a third node (C) and having gates connected in common and connected to the first node; a second inverter circuit comprising a PMOS transistor (P1) and an NMOS transistor (N1) connected in series between the power supply potential and the third

node (C) and having gates connected in common and connected to the second node; and a third NMOS transistor (N3) having a drain and source connected between the third node (C) and the ground potential, and a gate connected with the control signal, wherein the control signal is set to a predetermined level in an initial state to precharge the first and second nodes, and thereafter a molten state of a fuse mounted to the fuse mounting section is detected in accordance with a potential level of the second node (B) at a change in the level of the control signal.